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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,476	05/17/2005	Andrea Bragagnini	23301	3939

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EXAMINER	
ROCHE, JOHN B	
ART UNIT	**PAPER NUMBER**
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,476	BRAGAGNINI ET AL.	
	Examiner	Art Unit	
	John B. Roche	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *8-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/17/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

The disclosure is objected to because of the following informalities:
On page 15, line 29, "mastering" should read –masterin-.

Appropriate correction is required.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 8-10 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claims have not been further treated on the merits.

Claims 1-4 are objected to because of the following informalities:

In claim 1, line 12, "buffer" should read –buffers-.

In claim 1, lines 14 and 15, "modules" should read –module-.

In claim 1, line 22, "IDMA" should read –DMA-.

In claim 1, line 30, "data;" should be followed by –and-.

In claim 2, line 6, "buffers;" should be followed by –and-.

In claim 5, line 14, "transfers" should read –transfer-.

In claim 6, line 3, "transfers" should read –transfer-.

In claim 6, line 5, "block" should read –blocks-.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Walker et al. (US 2003/0033454), hereafter referred to as Walker et al.'454.

Referring to claim 1, Walker et al.'454 anticipates a method of exchanging data within a direct memory access arrangement including a plurality of IP blocks (dedicated modules, paragraph 9, line 3), comprising the steps of: associating with said IP blocks respective DMA modules (DMA ports A through D, paragraph 30, line 4), each of said DMA modules including an input buffer (data is buffered internally between read and write operations, paragraph 4, lines 6-7) and an output buffer (data is buffered internally between read and write operations, paragraph 4, lines 6-7); coupling said DMA modules over a data transfer facility (coupled to one or more buses, paragraph 9, lines 2-3) in a chain arrangement, wherein each said DMA module, other than the last in the chain,

has at least one of its output buffers coupled to the input buffer of another said DMA module downstream in the chain (up to 16 possible options for connectivity, paragraph 30, lines 7-8) and each said DMA module, other than the first in the chain, has its input buffer coupled to the output buffer of another of said DMA modules upstream in the chain (up to 16 possible options for connectivity, paragraph 30, lines 7-8); causing each of said DMA modules to interact with the respective IP block by writing data from the input buffer of the IDMA module into the respective IP block (writing data to destination, paragraph 4, line 3) and reading data from the respective IP block into the output buffer of the DMA module (reading data from source, paragraph 4, line 2); and operating said input and output buffers in such a way that: said writing of data from the input buffer of the DMA module into the respective IP block is started when said input buffer is at least partly filled with data (it is inherent to the invention that the buffer be at least partly filled with data while writing into the IP block); when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain (couple port A to port B, paragraph 30, line 8) or, in the case of the last DMA module in the chain, are provided as output data (ports coupled to other locations, paragraph 24, lines 1-2).

Note that claim 5 contains the corresponding limitations of claim 1 as shown above; therefore, it is rejected using the same reasoning accordingly.

As to claim 2, Walker et al.'454 also anticipates the steps of associating to said output buffers and input buffers coupled in the chain at least one intermediate block to

control data transfer between said coupled buffers (FIFO buffer, paragraph 38, line 16); and controlling transfer of data between said coupled buffers over said data transfer facility by: issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of: data existing to be transferred and enough space existing for receiving said data when transferred (DMA modules cannot function properly unless there is a method to confirm that data exists to be transferred and/or enough space exists for receiving the transferred data); issuing at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met (bit 8 in transfer size configuration register set to 1, paragraph 37, line 1); and transferring data between said requesting buffer and said coupled buffer (transfer process initiated, paragraph 37, line 2), whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement (read requests can still be made despite busy memory/module, paragraph 38, lines 23-25).

As to claim 3, Walker et al.'454 also anticipates including a CPU in the arrangement (processor 7, paragraph 33, line 1); and using said CPU for transferring data to be processed into the input buffer of the first DMA module in said chain (processor 7 issues a data instruction to DMA controller 5 and writes the source address to the source configuration register, paragraph 33, lines 1-5); and using said CPU for collecting said output data from the output buffer of the last DMA module in said chain (processor 7 issues a data instruction to DMA controller 5 and writes the destination address to the destination configuration register, paragraph 33, lines 1-5).

As to claim 4, Walker et al.'454 also anticipates configuring said DMA modules via said CPU (processor 7 issues data transfer instructions containing source address and destination address to DMA controller 5, paragraph 33, lines 1-4).

As to claim 6, Walker et al.'454 also anticipates that at least one of said input and output buffers has a fixed data width with respect to said data transfer facility (consistent data width regarding bus transfers is inherent to proper functionality of DMA modules) and a selectively variable data width with respect to said respective IP blocks (variable buffer size parameters bits 4:2 in source and destination configuration registers, paragraph 33, line 10 – paragraph 34).

As to claim 7, Walker et al.'454 also anticipates a slave interface module (processor 7, paragraph 33, line 1) configured for reading from outside the architecture data relating to at least one parameter selected from the group consisting of how many bits are available in said input buffer (size of the data block to be transferred, paragraph 36, lines 1-2); how many bits are present in said input buffer (destination address register buffer size bits 4:2, paragraph 34); how many bits are available for reading in said output buffer (source address bits 31:10, paragraph 33, line 10); and how many bits are present in said output buffer (source address register buffer size bits 4:2, paragraph 33, line 10).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pandya (US 2004/0010612), hereafter referred to as Pandya'612, teaches an IP processor that uses remote direct memory access to facilitate the processing and inspection of IP packets.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Roche whose telephone number is 571-270-1721. The examiner can normally be reached on M-F, 7:30 AM – 4:00 PM EST/EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JR

JR

HENRY TSAI
SUPERVISORY PATENT EXAMINER

8/20/07